DKTE Society's

TEXTILE & ENGINEERING INSTITUTE

(An Autonomous Institute)

Rajwada , Ichalkaranji 416115

DEPARTMENT: ELECTRONICS ENGINEERING

CURRICULUM

Master of Technology Program(Electronics)

First Year

With Effect From

2017-18

Teaching and Evaluation Scheme for
First Year M.Tech Programme in Electronics Engineering
Semester-I

Sr No	Course Code	Name of the Course	Group	Teaching Scheme				Credits
				Theory Hrs/ Week	Tutorial Hrs/ Week	Practical Hrs/ Week	Total	
1	ELL526	Advanced Digital Signal Processing	D	4	0	0	4	4
2	ELL527	Advanced CMOS VLSI Design	D	4	0	0	4	4
3	ELL528	Random Signal Processing	D	3	1	0	4	4
4	ELL55*	Elective-I	D	3	1	0	4	4
5	ELL56*	Elective II	D	3	1	0	4	4
6	ELL535	Research Methodology	C,F	2	0	0	2	2
7	ELP536	Advanced Digital Signal Processing lab	D	0	0	2	2	2
8	ELP537	Advanced CMOS VLSI Design Lab	D	0	0	2	2	2
9	ELD538	Seminar-I	F	0	0	2	2	2
Total				**19**	**3**	**6**	**28**	**28**

Group Details Abbreviations
A: Basic Science
B: Engineering Science
C: Humanities Social Science & Management
D: Professional Courses & Professional Elective
E: Open Elective
F: Seminar/Training/ Project

Course Code Abbreviations
L: lecture course
P: Laboratory based course
I:Self study

Elective I- ELL55*	
ELL529	Advanced Digital Image Processing
ELL530	Design of Digital Circuits & Logic Design
ELL531	Advance communication Systems

Elective II- ELL56*	
ELL532	Advanced Computer Architecture
ELL533	Digital Design using Verilog
ELL534	High Performance Communication Networks

First Year M.Tech Sem-I

ELL526: Advanced Digital Signal Processing

Teaching Scheme	
Lectures	4 Hrs/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites-Digital Signal Processing

Course Objectives

1. To cover the basic theory and algorithms that are widely used in signal processing
2. To design adaptive filters using different algorithms
3. To develop linear predictive model.
4. Understand multirate digital signal processing
5. Compute power spectral estimation of signals.
6. Make comfortable with wavelet transform and its applications.
7. Understand speech processing.

Course Outcomes

At the end of the course students will be able to

1. Appropriately select and design digital filter satisfying given specification
2. Analyze signals using wavelets, filter banks, and multi-resolution techniques
3. Apply theoretical understanding to identify applications to use different adaptive filtering approaches.
4. Analyze the effect of up-sampling and down-sampling operations on a signal
5. Use various techniques to determine the power spectral density of a signal
6. Compute speech parameters using LPC & Cepstrum techniques.

Course Contents

Unit 1. **Design of Digital Filters:** **9 Hrs.**

Design of optimum equiripple linear phase FIR filters, Design of FIR differentiator, Design of Hilbert transformers, Pade approximation method, Least squares Design methods, FIR Least- Squares Inverse Filters.

Unit 2. **Wavelet Transforms for Signal Processing:** **10 Hrs.**

Introduction to wavelet transform, Time frequency resolution, Heisenberg's Uncertainty Principle, The Continuous Wavelet Transform – scaling – shifting – scale and frequency – The Discrete Wavelet Transform – One Stage filtering – Approximation and Details – Filter bank analysis – multi resolution formulation of wavelet systems – Number of levels – Wavelet reconstruction – Reconstruction filter- Reconstructing Approximations and details, Applications in compression and denoising.

Unit 3. **Adaptive systems :** **9 Hrs.**

Definitions and characteristics - applications - properties- Wiener – Hopf equation- Searching performance surface- gradient estimation - performance penalty - LMS algorithm- sequential regression algorithm - adaptive recursive filters

Unit 4. **Fundamentals of Multirate Theory:** **9 Hrs.**

The sampling theorem revisited, Basic Multirate operations- Decimation and Interpolation - Digital Filter Banks- DFT Filter Bank- Identities- Polyphase representation

Maximally decimated filter banks: Polyphase representation - Errors in the QMF bank- Perfect reconstruction (PR) QMF Bank

Unit 5. **Spectral Estimation:** **10 Hrs.**

Power spectral density and energy spectral density, Estimation of spectra from finite duration signals, Nonparametric methods: Periodogram (Bartlett method), Modified periodogram (Welch method), Blackman-Tukey methods, Parametric methods: Use of AR model parameters for spectrum estimation Burg Methods, maximum entropy method.

Unit 6. **Speech Signal Processing** **9Hrs**

Digital models for speech production, LTI and LTV model, voiced/unvoiced decision making using ZCR and spectrum tilt, Pitch period estimation using autocorrelation method and average magnitude difference function, pitch period measurement using spectrum domain: FFT based method, Cepstrum domain. Linear predictive Coding: Basic Principles – formulation of LPC equation - solution of LPC equations – Durbin recursive solution. Formants and relation of formants with LPC.

Reference Books

1. John J. Proakis, Dimitris G. Manolakis, : Digital Signal Processing', Pearson Education, 2002.
2. Dr.Shaila D Apte, " Advanced Digital Signal Processing", Wiley Precise Textbook Series
3. Alan V Oppenheim, Ronald W Schafer, John R Back, Discrete Time Signal Processing, PHI, 2nd Edition 2000.
4. Dr.Shaila D Apte, " Speech and Audio Processing", Wiley Precise Textbook Series
5. S.Salivahanan, A.Vallavaraj, Gnanapriya, Digital Signal Processing, McGraw-Hill / TMH, 2000.
6. E.C.IfeachorBarrie,W.Jervis,"Digital Signal Processing", Pearson Education. Second Edition
7. Raghuveer. M. Rao, AjitS.Bopardikar, Wavelet Transforms, Introduction to Theory and applications, Pearson Education, Asia, 2000

First Year M.Tech. Sem-I
ELL527: Advanced CMOS VLSI Design

Teaching Scheme	
Lectures	4 Hrs. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Digital Circuit Design, Semiconductor Physics

Course Objectives

1. To gain knowledge on theory, design equations, characteristics of MOS and CMOS inverter, and to extend the concept to MOS switch, design of logic device
2. To understand the CMOS process and Technology
3. To gain knowledge on MOS models, transistor sizing, issues related to PDF and scaling concept and also to understand MOS circuit Simulation.
4. To design Combinational Logic Designs in CMOS and their layout.
5. To design sequential Logic Designs in CMOS and their layout.
6. To understand the design concepts of MOS based digital IC designs

Course Outcomes

At the end of the course students will be able to

1. Explain the theory, design equations, characteristics of MOS and CMOS inverter, and will design of logic device using CMOS
2. Explain CMOS process and Technology.
3. Compare MOS models, and explain transistor sizing, issues related to PDF and scaling
4. Design different combinational logic circuit designs and draw their layouts.
5. Design different sequential logic circuit designs and draw their layouts.
6. Explain design of basic Digital ICs

Course Contents

Unit 1. **Basics of CMOS :** **10 Hrs.**

VLSI Design: History, Trends, Quality Metrics of digital design, CMOS transistors (n-channel and p-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices, CMOS circuit analysis: MOS transistor static/switching characteristics, MOS device equations and capacitance Model, secondary and Short channel effects, CMOS inverter design equations and characteristics

Unit 2. **CMOS Process and Layout**: **6Hrs.**

CMOS Technologies, layout Design rules, p well / n well / twin well process layout examples on simple and complex logic circuits, stick diagram Calculations for Area of cell.

Unit 3. **Circuit Characterization & Design parameters:** **10 Hrs.**

Delay estimation, Delay models: RC delay model, Elmore Delay model, Transmission line model, Logical effort, Transistor Sizing, CMOS Inverter Power dissipation, PDP, Interconnect, The wire, Interconnect parameters (C, R, L). Technology Scaling, Basics of SPICE simulator, SPICE models for MOS transistor.

Unit 4. **Combinational Logic Designs in CMOS:** **9 Hrs.**

Static CMOS logic circuit design: Ratioed circuits; pseudo nMOS, Dynamic CMOS logic circuit Design: Domino Logic, NORA logic, Pass Transistor circuits, CMOS with Transmission Gates, Principles of drawing layouts of combinational logic circuits with examples.

Unit 5. **Sequential Logic Designs in CMOS:** **9 Hrs.**

Introduction to Sequential logic design, registers, Dynamic latches, Clock generation distribution: Clock generation, principles of clocked circuits, Timing issues in clocked circuits: Timing, Clock skew, clocking styles, Pipelining and its examples

Unit 6. **Digital IC Design:** **7Hrs**

Design Methodologies: Digital CMOS IC design: Implementation Strategies for Digital ICs, Sea of Gates (SoG) Cell based design, Full custom Design, SOC, design flow, design economics, CMOS Physical Design styles, Layout optimization.

Reference Books

1. "Digital Integrated Circuits", Rabey, Chandrakasan, Nikolic, Pearson Education, 2nd edition.
2. "Principles of CMOS VLSI Design", Neil Weste, Kamran Esharghian, Addison
3. "Essentials of VLSI Circuits and Systems", Kamran Eshraghian, Pucknell and Eshraghian, Prentice-Hall (India)
4. "CMOS Digital Integrated Circuits" .Analysis and Design", Kang, Leblebici, TATA McGRAW Hill.
5. "CMOS VLSI Design", Neil Weste, David Harris, Ayan Banerjee, Pearson Education, 3rd Edition, 2008.
6. "CMOS VLSI Design: A circuit and system perspective, Neil Weste, David Harris, Pearson Education, 4th Edition.
7. "Digital Integrated Circuits" Thomas A. DeMassa, Zack Ciccone, Wiley publication.

First Year M.Tech. Sem-I
ELL528: Random Signal Processing

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Maths-I, II and III, Signal Processing

Course Objectives

1. To perform statistical analysis of Random Variables.
2. To learn random processes.
3. To gain the knowledge of Markov chain and its properties.
4. To understand the Queuing theory

Course Outcomes

At the end of the course students will be able to

1. Apply the fundamentals of Probability theory

2. Solve engineering problems using probability theory, random variables, and random processes
3. Identify basic models of random processes and explain their use for the designing of components in various applications in the field of communication, signal processing etc.
4. Understand basic concepts in Markov processes.
5. Derive and Analyze queuing systems.

Course Contents

Unit 1. **Probability:** **8 Hrs.**

Definition of probability, Axioms of probability, theorems on probability of events, Laws of probability, Conditional probability, Independents of events, Burnoli'strial, Baye's theorem.

Unit 2. **Random Variables**: **10 Hrs**

Introduction and definition of random variables, Probability/Cumulative distribution function, Properties of distribution function, Probability density functions, Properties of Probability density functions. Uniform, Gaussian, Exponential random variables, Estimation of mean expected value & variance.

Unit 3. **Two dimensional Random Variables:** **10Hrs**

Introduction and Definition of a Two dimensional Random Variables, Probability / Cumulative Distribution Function of a Two dimensional Random ,Probability Density Functions of a Two dimensional Random, Marginal Distribution function & Marginal Density Functions

Unit 4. **Random Processes:** **10 Hrs.**

Basic Definitions and Important Random Processes, Useful classifications of Random Process , Types of Random Processes, strict sense stationary Processes, Wide- sense stationary Processes, Properties of Auto-correlation & Cross- correlation.

Unit 5. **Markov Chains:** **8 Hrs.**

Introduction , Definition of Markov Chains , Transition Probability Matrix, Transition Diagram, Homogenous Markov Chains, Chapman-Kolmogorvov Equation, Classification of states, Semi -Markov Chains, Waiting time for A Change of state, Counting Process, Poisson Process, Properties of Poisson Process.

Unit 6. **Queuing Theory** **7 Hrs**

Introduction, Cost Equation, steady state probability, Exponential models, Network of queues, The system M/G/1.

Reference Books

1. *"Introduction to Probability Models",* Sheldon M. Ross,Elsevier, Third edition
2. "*Introduction to Probability and Random Processes*" Jorge L. Aunin , V. Chandrasekar, McGraw Hill
3. *"Random Signal Analysis"*G.V.Kumbhojkar., Pradhnya Publications
4. *"Probability &Queueing Theory"* Dr. P..Kandasamy, Dr.K.ThilagavathiDr.K.Gunavathi,.S.Chand publishing & Co.
5. *"Random Processes, Filtering, Estimation & Detection"* Lonnie C. Ludeman, Wiley India Pvt Limited

First Year M.Tech. Sem-I
ELL55*- Elective-I: ELL529- Advanced Digital Image Processing

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites-Maths-I, II and III, Digital Signal Processing, Digital Image Processing.

Course Objectives

1. To understand the mathematical fundamentals for 2-D transforms
2. To learn and compare the 2-D image transforms.
3. To learn image filtering and enhancement operation.
4. To understand concepts of colour models and colour image processing
5. To understand different image analysis techniques

Course Outcomes

At the end of the course students will be able to

1. Realize the importance of mathematical fundamentals of 2-D transforms.
2. Compare transform-domain representation of images based on Fourier, DCT, Haar, etc.

3. Discuss the 2-D filtering techniques in image enhancement and image restoration
4. Conduct independent study and analysis of different color models and processing .
5. Choose suitable features and the associated techniques for image analysis

Course Contents

Unit 1. Introduction **8 Hrs.**

2-D systems, Mathematical preliminaries-Fourier Transform, Z-Transform, optical and modulation transfer function, Matrix theory, Random signals, discrete Random Fields, Spectral density function.

Unit 2. Image Transforms: **9 Hrs.**

Introduction, 2-D orthogonal & unitary transforms, Properties of unitary transforms, DFT,DCT, DST, Hadamard, Haar, Slant, KLT

Unit 3. Image Filtering & Restoration: **9 Hrs.**

Image observation models, Inverse & Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation & geometric correction.

Unit 4. Color and multispectral image processing **8 Hrs.**

Color and multispectral image processing Color Image-Processing Fundamentals, RGB Models, HSI Models, Relationship Between Different Models. Multispectral Image Analysis - Color Image Processing.

Unit 5. Image Analysis I: **8 Hrs.**

Edge detection-First and second order edge detection operators, Thresholding, Region growing, Fuzzy clustering, Watershed segmentation algorithm, Active contour methods, Texture feature based segmentation, Model based segmentation.

Unit 6. Image Analysis II: **10Hrs**

Localized feature extraction, detecting image curvature, Hough transform, shape skeletonization, Boundary descriptors, Moments, shape features, Texture descriptors- Autocorrelation, Co-occurrence features, Run length features, Principal component, Fractal model based features, Local Binary Pattern.

Reference Books

1. "Digital Image Processing", Gonzalez and Woods, Pearson Publication. 3rd Edition
2. Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press, 2008.

3. Anil K. Jain, Fundamentals of Digital Image Processing, Pearson Education,Inc., 2002

4. "Digital Image Processing" Willium K. Pratt Wiley, 3rd Edition.
5. Digital Image Processing", K.R. Castlemann, Pearson Publication

6. "Image Processing, Analysis and Machine Vision", Milan Sonka, Roger Boyle, PWS Publishing.

First Year M.Tech. Sem-I
ELL55*- Elective-I: ELL530-Design of Digital Circuits and Logic Design

Teaching Scheme	
Lectures	3 Hrs /Week
Tutorial	1 Hrs. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Digital System Design

Course Objectives

1. To learn state of the art techniques and algorithms for synthesis and minimization of digital systems
2. To design different architectural synthesis to optimize combinational and sequential machine design
3. To identify and analyse fault detection by experimentation

Course Outcomes

At the end of the course students will be able to

1. Understand concept of digital circuits design approach
2. analyse the reliable design and fault detection of digital circuits by using threshold logic concepts
3. design and synthesize the digital circuits with capabilities ,minimization and transformation of different sequential machines
4. design algorithms to identify state of digital circuits and detect faults
5. design logic circuits for hardware testing using design for testability like boundary scan and BIST

Course Contents

Unit 1.	**Digital system design**: Building block circuits, Flip flops and registers with enable input, SRAM, SRAM blocks in PLDs, design of bit counting circuit, shift and add multiplier, divider, clock synchronization, clock skew, switch denouncing, synchronous inputs to flip flops	**8 Hrs.**
Unit 2.	**Threshold Logic**: Introductory Concepts, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits, Boolean Differences, Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic	**8 Hrs.**
Unit 3.	**Capabilities, Minimization, and Transformation of Sequential Machines**: The Finite- State Model, Capabilities and Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines. Moore type FSMs, serial adder, Mealy type And Moore type, Asynchronous sequential circuits, analysis and synthesis, state reduction, state assignments, Hazards-static and dynamic, a complete design example for vending machine controller	**11 Hrs.**
Unit 4.	**Structure of Sequential Machines**: Introduction, Example, State Assignments using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, Decompositions	**9 Hrs.**
Unit 5.	**State—Identifications and Fault-Detection Experiments**: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault-Detection Experiments, Design of Diagnosable Machines Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection Experiments for Machines which have no Distinguishing Sequences	**9 Hrs.**
Unit 6.	**Design for testability** Hardware testing and design for testability: Testing combinational and sequential logic, scan testing, boundary scan and BIST	**7 Hrs.**

Reference Books

1. ZviKohavi, "Switching and Finite Automata Theory", 2nd Edition. Tata McGraw Hill Edition
2. Charles Roth Jr., "Digital Circuits and logic Design",

3. Parag K Lala, "Fault Tolerant and Fault Testable Hardware Design", Prentice Hall 1985
4. E. V. Krishnamurthy, "Introductory Theory of Computer", Macmillan Press Ltd, 1983
5. Mishra & Chandrasekaran, "Theory of Computer Science – Automata, Languages and Computation", 2nd Edition, PHI,2004

First Year M.Tech. Sem-I
ELL55*- Elective-I: ELL531-Advance Communication Systems

Teaching Scheme	
Lectures	3 Hrs /Week
Tutorial	1 Hr. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites- Digital Communications, Random Signal Processing, Engineering Mathematics-III

Course Objectives

1. Explain the system structure of analogue and digital communication systems
2. Use mathematical tools to analyze the performance of communication systems
3. Use probability theory and stochastic processes in communication system applications.

Course Outcomes

At the end of the course students will be able to

1. Acquire knowledge about Switching Systems.
2. Acquire knowledge about Traffic Engineering.
3. Ability to identify, formulate and solve engineering problems related to Satellite communication and remote sensing

Course Contents

Unit 1 **Equalization** **7 Hrs.**

Linear Equalization, Decision feedback equalization, iterative equalization and decoding, adaptive equalization.

Unit 2 **Co channel and non co channel interferences** **9 Hrs.**

Propagation path loss and mobile point to point models, Co-channel & Non-cochannel interference, Exploring co-channel interference areas in

system, reduction of cochannel interference, Different types of non-co-channel interferences, different ways to reduce interference and in turn improve cell coverage

Unit 3 **Mobile Telephony** **10 Hrs.**

Circuit switched data services- HSCSD**,** Packet switched data services- GPRS, CDPD, EDGE, Introduction to GSM systems, GSM architecture, GSM network structure, Cell layout and frequency planning, Mobile station, Base station systems, Switching subsystems, Home location registers, VLR (Visiting location registers), Equipment identity register, Echo canceller, CDMA : Introduction to code division multiple access technology, IS 95: system Architecture, Spread spectrum systems: System architecture for wireless communication , Diversity, Combining and antennas, Physical and Logical channels of IS 95 CDMA, Voice application in CDMA systems

Unit 4 **Multiuser Radio Communications** **9 Hrs.**

Multiple-Access Techniques, Satellite Communications, Radio Link Analysis, Wireless Communications, Statistical Characterization of Multipath Channels, Types of fading channels, TDMA & CDMA Wireless Communication System, Source Coding of Speech for Wireless Communication, Adaptive Antenna Arrays for Wireless Communication, Equalizer

Unit 5 **MIMO** **7 Hrs.**

Introduction to MIMO, MIMO Channel Capacity, SVD and Eigen modes of the MIMO Channel, MIMO Spatial Multiplexing - BLAST, MIMO Diversity - Alamouti, OSTBC, MRT, MIMO – OFDM

Unit 6 **Radar Systems** **10Hrs**

The Radar Equation, Detection of Signal in Noise, Integration of Radar Pulses,Transmit Power, Pulse Repetition frequency, system losses, Antenna Parameters and Radar Equation consideration,MTI and Pulse Doppler Radar, Doppler Filter Banks, Digital MTI Processing Detector, Pulse Doppler Radar,Tracking Radar, Monopulse Tracking, Conical Scale and Sequential Lobbing,Comparison of Trackers, Automatic tracking with Surveillance Radar

Reference Books:

1. Bernard Sklar, Digital Communcation: Fundamentals and applications, Pearson Education Asia Edition
2. Theodore S. Rappaport, "Wireless communications, principles and practices", Pearson Education.
3. Skolnik, "Radar Systems".

4. V.K.Garg, "IS-95 CDMA & CDMA 2000", Pearson Education.
5. B. P. Lathi, "Modern Digital and Analog Communications Systems", Oxford.
6. Shu Lin, Daniel J. Costello, "Error Control Coding", Pearson Education.
7. S. P. Eugene Xavier, "Statistical Theory of Communication", New Age International Publishers.
8. William C.Y.Lee, "Mobile Cellular Telecommunications Analog and Digital Systems", II Ed. TMH.
9. Todd. K. Moon , "Error Correcting Codes".

First Year M.Tech. Sem-I
ELL56*- Elective-II: ELL532-Advanced Computer Architecture

Teaching Scheme	
Lectures	3 Hrs /Week
Tutorial	1 Hr. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Computer Organization, Operating Systems

Course Objectives

1. To understand architecture of advanced computers.
2. To study various techniques to improve the performance of an advanced computer system.
3. Study and understand architecture of multicore computers such as ARM11 MPC core 699.
4. Study Memory Hierarchy Design.

Course Outcomes

At the end of the course students will be able to

1. Understand the basic principles of operation of Advance Computes.
2. Understand various advanced techniques to improve the performance of computer system.
3. Understand the operations of multicore computers.
4. Analyse performance of computer based on memory technology and its optimization.

Course Contents

Unit 1. **Pipelining and ILP** **8 Hrs.**

Fundamentals of computer design-Measuring and reports performance - Instruction level parallelism and its exploitation –Concepts and challenges- Overcoming data hazards with dynamics scheduling –Dynamic branch prediction- Speculation- Multiple issue processors- Case studies.

Unit 2. **Advanced Techniques for Exploiting ILP** **8 Hrs.**

Complier techniques for exposing ILP –Limitation on ILP for realizable Processors –Hardware versus software speculation

Unit 3. **Multithreading** **7 Hrs.**

Using ILP support to exploit thread –level parallelism- performance and efficiency in advanced multiple issue processors- Case studies.

Unit 4. **Multiprocessors** **8 Hrs.**

Symmetric and distributed shared memory architectures – Cache coherence issues –Performance issues-Synchronization issues- Models of memory consistency – Interconnection networks – Buses, crossbar and multi –stage switches.

Unit 5. **Multicore Computers** **10 Hrs.**

Hardware performance issues, Software performance issues, Multicore organization, Intel x 86 multicore organizations, ARM11 MPC core 699.

Unit 6. **Memory Hierarchy Design** **9Hrs**

Introduction – Optimization of cache performance – Memory technology and optimization – introduction: Virtual memory and virtual machines – Design of Memory hierarchies – Case studies.

Reference Books

1. John L. Hennessey & David A. Patterson," Computer Architecture-A quantitative approach", Morgan Kaufmann/ Elsevier, 4th. Edition, 2007.
2. David E.Culler,Jaswinder pal Singh, "parallel computing architecture : A hardware / software approach ", Morgan Kaufmann / Elsevier ,1997.
3. William Stallings, " Computer organization and Architecture- Designing for performance ",Pearson education , 8th Edition ,2006

First Year M.Tech. Sem-I
ELL56*-Elective-II: ELL533- Digital Design using Verilog

Teaching Scheme	
Lectures	3 Hrs /Week
Tutorial	1 Hr. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites- Digital Design

Course Objectives

1. To learn the concepts of modeling a digital system using Verilog hardware description Language
2. To study Hierarchy and modelling of structures Behavioural and register transfer level modelling and Write RTL Verilog code for synthesis
3. To understand the concept of user defined functions, tasks, delays, test benches, timing checks
4. To study the Verilog models for memory, buses and I/O interfacing.
5. To learn Design methodology of HDL

Course Outcomes

At the end of the course students will be able to

1. Apply concepts of modeling a digital system using Verilog hardware description Language
2. Explain the Hierarchy and modelling digital circuits using Verilog.
3. Implement user defined functions, tasks, delays, test benches, timing checks using hardware description language
4. Build the Verilog models for memory, buses and I/O interfacing.
5. Explain Design methodology of HDL

Unit No.	**Course Contents**	
Unit 1	**Introduction to Verilog:** Verilog as HDL, Simulation and Synthesis Tools, Test Benches. **Language constructs and conventions,** , Parameters, Memory, Operators, System Tasks.	**10Hrs**
Unit 2	**Gate level modeling:** Design of Basic Circuits**,** Data flow level modeling: assignments and operators, Behavioral modeling:*Wait* construct, The case statement, Simulation Flow.	**10Hrs**

	i*f* and i*f*-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, whileloop, forever loop ,whileloop, forever loop, parallel blocks,force-release construct, Event.	
Unit 3	**Functions, tasks, and u ser-defined primitives:** Introduction, Function, Tasks, User- Defined Primitives (UDP), FSM Design (Moore and Mealy Machines). **System tasks, functions and compiler directives:** Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General observations.	**10Hrs**
Unit 4	**Verilog models for memories and buses:** Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity Static RAM Memory, A simplified 486 Bus Model, UART Design.	**10Hrs**
Unit 5	**Processor Basics and I/O interfacing,** Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **I/O interfacing:** I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software	**8Hrs**
Unit 6	**Design Methodology:** Design flow, Design optimization, Design for test,	**4Hrs**

TEXT BOOKS:

1. T.R. Padmanabhan and B. Bala Tripura Sundari, "*Design through Verilog HDL''*, WSE, IEEE Press 2008.
2. J. Bhaskar, *"A Verilog Primer''*, BSP, 2nd edition 2003.
3. Peter J. Ashenden **"***Digital Design: An Embedded Sytems Approach Using VERILOG",* Elesvier, 2010

REFERENCES:

1. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition,2003.Thomas and Moorby,
2. Thomas &Moorby's*"The Verilog Hardware Description Language"*, kluwer academic publishers, 5th edition, 2002.
3. Stephen Brown and ZvonkoVranesic, *"Fundamentals of Logic Design with Verilog"*, TMH publications, 2007.
4. Charles.H.Roth,Jr., Lizy Kurian John *"Digital System Design using VHDL"* , Thomson, 2nd Edition, 2008

First Year M.Tech. Sem-I
ELL56*- Elective-II: ELL534-High Performance Communication Networks

Teaching Scheme	
Lectures	3 Hrs /Week
Tutorial	1 Hr. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Computer communication network, Broadband communication

Course Objectives

1. To understand the operation of Ethernet ,Token Ring & Wireless LAN
2. Describe the structure of ISDN & BISDN
3. Study and understand ATM & Frame Relay
4. Study and understand Optical Networks

Course Outcomes

At the end of the course students will be able to

1. Understand the operation of Ethernet ,Token Ring & Wireless LAN
2. Understand the basic principles ISDN & BISDN.
3. Understand the operation of ATM & Frame Relay
4. Learn and understand working of Optical Networks

Course Contents

Unit 1. **PACKET SWITCHED NETWORKS** **7 Hrs.**

OSI & IP models – Ethernet (IEEE 802.3) – Token Ring (IEEE 802.5) Wireless LAN (IEEE 802.11), bluetooth technology**O**verview, protocol stack, link manager, Host controller interface, Service discovery protocol, WAP Applications, encryption and security, QoS.

Unit 2. **ISDN & Broadband ISDN and Optical Networks** **9 Hrs.**

Optical Links, WDM system, Optical cross-connects, Optical LANs, Optical paths and networks ISDN – overview –interfaces and functions- Layers and Services – Signalling System 7- Broadband ISDN architecture and protocols

Unit 3. **ATM And Frame Relay** **9 Hrs.**

ATM: Main features – addressing- signalling& routing, ATM header structure – adaptation layer – management & control – ATM switching & transmission.

Frame relay Protocols & services – congestion control – internetworking with ATM – Internet and ATM – Frame relay via ATM

Unit 4. **Switching Networks** **8 Hrs.**

Switching – Packet switching - Ethernet, Token Ring, FDDI, DQDB, Frame Relay, SMDS, Circuit Switched – SONET, DWDM, DSL, Intelligent Networks – CATV, ATM – Features, Addressing Signalling & Routing, Header Structure, ATM Adaptation layer, Management control, BISDN, Internetworking with ATM.

Unit 5. **Multimedia Networking Applications** **7 Hrs.**

Streaming stored Audio and Video, Best effort service, protocols for real time interactive applications, Beyond best effort, scheduling and policing mechanism, integrated services, RSVP- differentiated services

Unit 6. **Advanced Network Architecture** **10Hrs**

IP forwarding architectures overlay model –Multi protocol Label switching (MPLS) – integrated services in the Internet – Resource Reservation Protocol (RSVP) Differentiated services, Application Layer Protocols: FTP – File access and transfer, Online shared access, sharing by file transfer, The Major view of FTP TFTP, SMTP, and HTTP.

Reference Books:

1. High performance communication networks", 2ndedition by Jean Walrand, PravinVaraiya, Morgan Kaufmann Publication. (CH-1, 4)
2. "ISDN and Broadband ISDN with Frame Relay and ATM" 4th Edition by William Stallings, Pearson.(CH- 2,4)
3. "Bluetooth connect without cables" by Jennifer Bray and Charles Sturman , Pearson education Asia, LPE.(CH-1)
4. "Communication Networks-Fundamental concepts and Key architectures" by Leon Gracia, IndraWidjaja, McGraw Hill Companies.(CH- 6)
5. "Data Communications and Networking" 4th Edition by BehrouzForouzan, McFraw Hill Companies. (CH-3, 4)
6. Aunurag Kumar, D. Manjunath, Joy Kuri, "Communication Networking", Morgan Kaufmann Publishers, 2011. (CH-5)
7. J.F. Kurose & K.W. Ross, "Computer Networking- A Top Down Approach Featuring the Internet", Pearson, 2nd Edition, 2003. (CH-3, 4)

8. Nader F.Mir, "Computer and Communication Networks", Pearson Education, 2009. (CH-5)
9. Walrand .J. Varatya, "High Performance Communication Network", Morgan Kaufmann
Harcourt Asia Pvt. Ltd., 2nd Edition, 2000

First Year M.Tech. Sem-I
ELL535: Research Methodology

Teaching Scheme	
Lectures	2 Hrs. /Week
Total Credits	2

Evaluation Scheme	
SE-I	-
SE-II	-
SEE	-
CIE	**50**
Total	**50**

Course Objectives

1. To get introduced to research philosophy and processes in general.
2. To be able to formulate the problem statement and prepare research plan for the problem
3. To gain knowledge on Methods of Data Collection, Sampling and learn to apply various techniques for data analysis.
4. Appreciate the components of scholarly writing keeping in view ethical dimension and issues related with its quality

Course Outcomes

At the end of the course students will be able to

1. Explain some basic concepts of research and its methodologies
2. Investigate research problem and parameters
3. Able to demonstrate the ethics of research
4. Prepare a project proposal, write a research thesis, and paper

Course Contents

Unit 1. Objectives and types of research: **4 Hrs.**

Motivation and objectives : Introduction Concepts of Research, Meaning and Objectives of Research, Research Process, Criteria of Good Research, Research Problem Research methods vs Methodology, Types of research- Descriptive vs. Analytical, Applied vs. Fundamental, Quantitative vs. Qualitative, Conceptual vs. Empirical.

Unit 2. **Research Design:** **6 Hrs.**

Defining and formulating the research problem, Selecting the problem, Necessity of defining the problem, Importance of literature review in defining a problem, Literature review: Primary and secondary sources – reviews, treatise, monographs-patents, web as a source– searching the web -,Critical literature review-Identifying gap areas from literature review, Development of working hypothesis.

Unit 3. **Methods of Data Collection, Sampling and analysis of data** **8 Hrs.**

Data Collection: Primary data and Secondary Data, methods of primary data collection, classification of secondary data, designing questionnaires and schedules.

Sampling: Probability sampling: simple random sampling, systematic sampling, stratified sampling, cluster sampling and multistage sampling. Non-probability sampling: convenience sampling, judgment sampling, quota sampling. Sampling distributions.

Analysis of data: Statistical measures and their significance: Central tendencies, variation, skewness, Kurtosis, time series analysis, correlation and regression, Testing of Hypotheses: Parametric (t, z and F) Chi Square, ANOVA.

Unit 4. **Research proposal, Thesis writing and Paper Writing** **7 Hrs.**

Format of research proposal: Individual research proposal, Institutional proposal, Proposal of a student, Principles of Thesis Writing, Formats of Report Writing & Publication in Research Journals, impact factor of Journals, Ethical issues related to publishing, Plagiarism and Self-Plagiarism.

Reference Books

1. Research Methodology: An Introduction for Science & Engineering Students', by Stuart Melville and Wayne Goddard
2. 'Research Methodology: An Introduction' by Wayne Goddard and Stuart Melville
3. 'Research Methodology: A Step by Step Guide for Beginners', by Ranjit Kumar, 2nd Edition
4. 'Research Methodology: Methods and Techniques', by Dr. C. R. Kothari, New Age International Publisher
5. Research Methodology, G.C. Ramamurthy, Dream Tech Press, New Delhi
6. 'Management Research Methodology' by K. N. Krishnaswamy, AppaIyerSivakumar& M. Mathirajan, Person Education.
7. Software Engineering by Pressman

First Year M.Tech. Sem-I
ELP536: Advanced Digital Signal Processing Lab

Teaching Scheme		Evaluation Scheme		
ELL526: Practical	2 Hrs. /Week	CIE	ELL526	50
ELL55*: Tutorial Comprehensive Viva voce	1 Hr/week		ELL55*	50
		SEE	ELL526	25
			ELL55*	25
Total Credits	**2**	**Total**		**150**

Note: ELP536: Consists of Advanced Digital Signal Processing Lab POE external exam will be conducted for **ELL526 and** Comprehensive Viva voce of opted elective **ELL55***

List of Experiments based on ELL526: Advanced Digital Signal Processing

1. Program on FIR/IIR filter design
2. Program on FIR differentiator
3. Program on Hilbert transform
4. Implementation of Adaptive filtering algorithm
5. Predictive analysis of speech signal using LPC
6. Analysis of speech signal using Cepstrum
7. Program on Pitch period estimation using autocorrelation and average magnitude difference function method.
8. Program illustrating Multirate signal processing
    a. Implementing Decimator
    b. Implementing Interpolator
9. Program to implement sampling rate conversion by a factor of I/D
10. To find Power Spectral Density.
11. Simulink model for LMS Algorithm
12. Program on Continuous Wavelet transform
13. Program on application of Discrete wavelet transform

List of Tutorial Experiment to be performed based on opted ELL55*-Electives-I (**ELL529 OR ELL530 OR ELL531**)

List of tutorials Experiment based on ELL529-Advanced Digital Image Processing

List of tutorials to be performed on Matlab/ opencv

Sr.No	Name of Tutorial
1	Experiment on Fourier Transform
2	Experiment on demonstration of Singular Value decomposition
3	Implementation of Image filtering and restoration algorithms.
4	Study of impact different colour model in image processing.
5	Study of different edge detection operators and their comparison.
6	Experiment on Wavelet based segmentation.
7	Experiment on extracting the features using Fourier descriptor.
8	Experiment on extracting the features using moments.
9	Study of different gradient operators.
10	Experiment on Hough Transform.

First Year M.Tech. Sem-I

List of Tutorials: ELL530-Design of Digital Circuit and Logic Design

Tutorial to be conducted using VHDL

1. Design of digital clock generator
2. Design of combinational circuit
   - Adder(for fault analysis) using proteus
   - 4:1 mux with multiple i/p and o/p pins
3. Design of 4-bit ring counter
4. Design of Mod-6 counter
5. Pseudo Random Sequence Generator
6. Design of control unit8
   - Design of memory units
   - SRAM
7. Design of floating point arithmetic operations.
8. Study of 486 bus architecture.

First Year M.Tech. Sem-I
List of tutorial Experiments: ELL531 Advanced Communication Systems

List of Tutorials conducted using MatLab

Sr No	Name of the Tutorial
1	Perform Adaptive Equalization using MATLAB
2	Design an interference canceller using MATLAB
3	Study of GSM system using kit
4	Study of CDMA system using kit
5	Study of Adaptive Antenna Array using Simulation
6	Study of Eigen values, Eigen vectors and SVD of matrix using MATLAB
7	Study of Doppler radar using kit
8	Visit to Radar Station

First Year M.Tech. Sem-I
ELP537: Advanced CMOS VLSI Design Lab

Teaching Scheme		Evaluation Scheme		
ELL527: Practical	2 Hrs. /Week	CIE	ELL527	50
ELL528: Tutorial	1Hr/week		ELL528	50
			ELL56*	
ELL56*: Tutorial	1Hr/week	SEE	ELL527	25
			ELL528	25
			ELL56*	
Total Credits	**2**	**Total**		**150**

Note : ELP537 consists of **Advanced CMOS VLSI Design Lab: E**external Exam will be on POE of **ELL527** and comprehensive viva voce of **ELL528 & opted Elective ELL56*-- Elective II**

First Year M.Tech. Sem-I
List of Experiments: ELP537: Advanced CMOS VLSI Design

Experiment to be implemented using HDL(VHDL/Verilog)

1. Design and implementation of a) Full adder b) 4 bit counter
2. Design of shifter units

a) Conventional Shift Register b) Barrel Shifter.

3. Design of Sequential machine using FSM method

   a) Mealy Machine b)Moore Machine

4. Design and implementation of sequence detector

5. Design of Real Time VAT Process Control

Experiment to be implemented using Microwind/Mentor Graphics

6. Schematic and Layout implantation

   a) nMOS transistor b)pMOS transistor c)Resistor, Inductor, Capacitor

7. Schematic and Layout implantation

   a) Inverter and its Analysis
   b) Power Vs voltage
   c) Capacitances Vs Voltage
   d) Time Delay

8. Schematic and Layout implantation of

   a) NAND,NOR b) AND,OR

9. Schematic and Layout implantation

   a) XOR, XNOR
   b) Using Standard Circuit
   c) Using Transmission Gate

10. Layout implementation of MUX

    a) Basic Gates b) Transmission gate

11. Layout implementation

    a)Half adder b) Subtractor

12. Transmission Gate (TG)

    a) based 4:1 MUX

    b) TG based 3:8 Decoder c) TG based D and T Flip flops

    d) 3-bit Asynchronous counter using TG based T flip flop

    e) 3-bit SISO shift register using TG based D flip flop

NOTE: Comprehensive Viva Voce will be carried out by Internal and External examiners as oral examination for **ELL528**, Random Signal Processing and offered ELL56* -Elective-II subject (**ELL532, ELL533, and ELL534**)

First Year M.Tech. Sem-I

List of Tutorial Experiments: ELL533-Digital System Design using Verilog

Tutorial to be conducted using Verilog

1. Write a HDL code to describe the functions of a full adder using 3 modelling styles and verify using test bench

   A. Full adder data flow description

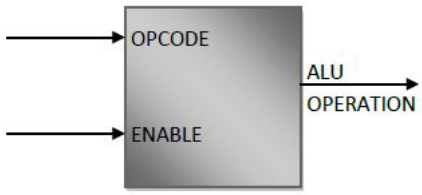
   B. Full adder behavioural description

   C. Full adder structural description

2. Design a 32-bit CLA and test it.

3. Write a model for 32 bit ALU using the schematic diagram given below, with A (31:0), B (31:0). ALU should use combinational logic to calculate an output based on the four-bit op-code input

OPCODE	ALU OPERATION
1.	A + B
2.	A – B
3.	A Complement
4.	A AND B
5.	A OR B
6.	A NAND B
7.	A XOR B



   ALU should pass the result to the out bus when enable line is high, and tri-state the out bus when the enable line is low. ALU should decode the 4 bit op-code according to the given in example below. Write the test bench to verify

4. Design 4 bit binary, BCD counters (synchronous reset and asynchronous reset) and "any sequence" counter and test the same.

   A. Binary synchronous reset 4 bit counter
   B. Binary asynchronous reset 4 bit counter

   C. BCD synchronous reset 4 bit counter

   D. BCD asynchronous reset 4 bit counter

   E. Binary any sequence up down 4 bit counter

5. Write the hardware description of a 8-bit register with shift left and shift right modes of operation and test its operation and verify using test bench

6. Write the hardware description of a serial adder with accumulator and verify using test bench

7. Write the hardware description of a 4-bit binary multiplier and verify using test bench
8. Write the hardware description of a 4-bit PRBS (pseudo-random binary sequence) generator using a linear feedback shift register and test it.
9. Write the hardware description of 1K RAM and test its operation
10. Write the hardware description for the system shown below. The first process should determine next state and control signals. The second process should update the registers on the rising edge of the clock.

First Year M.Tech. Sem-I
ELD 538: Seminar-I

Teaching Scheme	
Lectures	2 Hrs. /Student
Total Credits	2

Evaluation Scheme	
SE-I	-
SE-II	-
SEE	-
CIE	**50**
Total	**50**

Course Objectives

1. To make the student to know about his interest field
2. To understand the focusing and summing ability.
3. To develop the attitude towards research
4. To give an insight into forming problem statement
5. To improve the presentation skills

Course Outcomes

At the end of the course students will be able to

1. Appropriate and select seminar topic in his field of interest
2. Comprehend and summarize the topic studied
3. Analyze the topic and will explore further

4. Formulate the problem statement

5. Show improvement in confidence level

1. Each student will be required to prepare a Seminar Report and present a Seminar on a topic in any of the areas of modern technology related to Electronics Engineering including interdisciplinary fields.
2. The topic/title will be chosen by the student in consultation with the Faculty Advisor allocated to each student.
3. The student will be required to submit the Seminar Report and present a talk to an audience of Faculty/Students in open defense in front of the Seminar Evaluation Committee having faculty
4. Advisor as one of its members. The Head of Department will constitute the Seminar Evaluation Committee.

Continuous Internal Evaluation: CIE

1. Continuous evaluation of the seminar shall be made by guide.
2. The student is required to present the seminar-I which will be evaluated for 50 marks.

   The student shall submit the Seminar Report and present a talk to an audience of faculty/Students in open defense in front of the Seminar Evaluation Committee having Faculty Advisor as one of its members. This will **be evaluated for 50 marks**.

Teaching and Evaluation Scheme for

First Year M.Tech. Programme in Electronics Engineering

Semester-II

Sr. No	Course Code	Name of the Course	Group	Teaching Scheme				Credits
				Theory Hrs/ Week	Tutorial Hrs/ Week	Practical Hrs/ Week	Total	
1	ELL539	Real Time Embedded System design	D	4	0	0	4	4
2	ELL540	Analog & Mixed Mode VLSI Circuits	D	4	0	0	4	4
3	ELL541	Power Electronics Systems	D	3	1	0	4	4
4	ELL57*	Elective-III	D	3	1	0	4	4
5	ELL58*	Elective-IV	D	3	1	0	4	4
6	ELP 548	Real Time Embedded System design Lab	D	0	0	2	2	2
7	ELP 549	Analog & Mixed Mode VLSI Circuits Lab	D	0	0	2	2	2
8	ELD550	Mini Project-I/ Training/Seminar- II	F	0	0	2	2	2
Total				**17**	**3**	**6**	**26**	**26**

Group Details of Abbreviations

A: Basic Science
B: Engineering Science
C: Humanities Social Science & Management
D: Professional Courses & Professional Elective
E: Open Elective
F: Seminar/Training/ Project

Course Code Abbreviations

L: lecture course
P: Laboratory based course
I:Self study

Elective III- ELL57*	
ELL542	Advanced Image, Video Processing and applications
ELL543	Advanced Process Control
ELL544	Wireless Adhoc & Sensor Network
Elective IV- ELL58*	
ELL545	Artificial Neural Network
ELL546	VLSI in Digital Signal Processing
ELL547	Cryptography and Network Security

First Year M. Tech. Sem-II
ELL539: Real Time Embedded System design

Teaching Scheme	
Lectures	4 Hrs. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Digital Design, Microprocessor, Microcontroller

Course Objectives

1. To understand Embedded Computing.
2. To develop real-time algorithm for task scheduling.
3. To understand the working of real-time operating systems and real-time database.
4. To work on design and development of protocols related to real-time communication.

Course Outcomes

At the end of the course students will be able to

1. Explain the basics of embedded systems and the interface issues related to it
2. Able to develop real-time algorithm for task scheduling.
3. Explain the concepts of interrupts, hyper threading and software optimization.
4. Analyze the various Real Time OS by comparing different parameters.

Course Contents

Unit 1. EMBEDDED COMPUTING **7 Hrs.**

Complex systems and microprocessors, ARM Processor – CPU: Programming input and output, Supervisor mode, exception and traps, Assembly and Linking: Basic compilation techniques, Analysis and optimization of execution time, power, energy, program size – Program validation and testing

Unit 2. OVERVIEW OF OPERATING SYSTEM **9 Hrs.**

Basic Principles, Operating System structures, System Calls, Files, Processes – Design and Implementation of processes, Communication between processes, Concurrency: Principles of Concurrency, Mutual Exclusion H/W Support, software approaches, Semaphores and Mutex, Scheduling

Unit 3. **MEMORY & I/O MANAGEMENT** **9 Hrs.**

Memory Management requirements, Memory partitioning: Fixed, dynamic, partitioning Segmentation, Paging, Virtual Memory, Demand paging, Page Replacement Policies (FIFO, LRU, Optimal, clock), I/O Devices, Organization of I/O functions, Operating System Design issues, I/O Buffering.

Unit 4. **INTRODUCTION TO REAL TIME SYSTEM** **10 Hrs.**

Concept, Differences between General Purpose OS & RTOS, Model of Real Time System, Characteristics of Real Time System, Safety and Reliability, Types of Real Time Tasks, Timing Constraints, File systems, I/O Systems, Advantage and disadvantage of RTOS. POSIX standards, RTOS Issues - Selecting a Real Time Operating System, Comparative study of various RTOS.

Unit 5. **VXWORKS** **8 Hrs.**

VxWorks Scheduling and Task Management: Real time scheduling, Task Creation, Inter task Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts, I/O Systems: General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral, Case study using Vxworks

Unit 6. **RTOS APPLICATIONS** **8 Hrs.**

Case studies of simple applications of RTOS, RTOS for Image Processing, Embedded RTOS for voice over IP, RTOS for fault Tolerant Applications, RTOS for Control Systems.

Reference Books

1. Wayne Wolf, *"Computers as Components: Principles of Embedded Computing System Design,"* 2/e, Kindle Publishers, 2005.
2. Tanenbaum,*"Modern Operating Systems,"* 3/e, Pearson Edition, 2007.
3. Jean J Labrosse,*"Embedded Systems Building Blocks Complete and Ready-to-use Modules in C," 2/e, 1999.*
4. Raymond J.A.Bhur, Donald L.Bailey, *"An Introduction to Real Time Systems", PHI 1999.*
5. C.M.Krishna and G.Shin, *"Real Time Systems,"* McGraw-Hill International Edition, 1997.

First Year M.Tech. Sem-II
ELL540- Analog & Mixed Mode VLSI Circuits

Teaching Scheme	
Lectures	4 Hrs. /Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Analog Circuit Design, Digital Circuit Design

Course Objective

1. Understand the small and large signal models of CMOS transistors.
2. Exemplify single-stage and differential amplifiers and current mirrors
3. To gain knowledge on design basic operational amplifiers, understand the concept of gain, power, and bandwidth,
4. To learn concept of CMOS oscillators and PLL and data converters.
5. Design basic circuits using EDA tools

Course Outcomes

The student must at the end of the course be able to

1. Explain the significance of different biasing styles and apply them aptly for different circuits.
2. Design the basic building blocks like sources, sinks, mirrors and amplifiers
3. Comprehend the design of Op-amp.
4. Describe the concepts of CMOS oscillators and PLL and data converters
5. Design and use EDA tools for building and verify the basic analog circuits to tape-out including parasitic effects

Course Contents

Unit 1. **CMOS Amplifiers**: **11 Hrs.**

Review of basic MOS Device Physics: MOS I/V Characteristics, second order effects, MOS device models**,** CS stage with resistance load / MOS loads, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, Design aspects of all the above circuits.

Frequency response: CS stage, source follower, Common gate stage, Cascade stage and Difference pair

Unit 2.	**Differential Amplifiers:** Basic difference pair, common mode response, Differential pair with MOS loads and their design aspects, Gilbert cell.	**7 Hrs.**
Unit 3.	**Passive and active Current mirrors**: Current mirrors and design, Cascade mirrors, active current mirrors.	**7 Hrs.**
Unit 4.	**Operational Amplifiers:** Single stage OP-Amp Gain boosting, Common Mode Feedback, Slew rate, PSRR. Introduction to 2 stage OPAMP, Compensation of 2-stage OP-Amp.	**8 Hrs.**
Unit 5.	**Oscillators**: Ring Oscillators, VCO, Mathematical Model of VCO. **PLL:** Simple PLL, Charge pump PLL	**6 Hrs.**
Unit 6	**DATA converter architecture** :DAC Architectures, Resistors String, R-2R Ladder Networks, , Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.	**11 Hrs**

Reference Books

1 "Design of Analog CMOS Integrated Circuits", BehzadRazavi, TMH, 2007.

2 T.H. Lee " **The design of CMOS RF Integrated Circuits**" Cambridge University Press

3 Philip Allen, Douglas Holberg," **CMOS Analog Circuit Design"**, Oxford University, Press, 2011.

First Year M.Tech. Sem-II
ELL541: Power Electronics Systems

Teaching Scheme	
Lectures	4 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Power Electronics

Course Objectives

1. To provide the electrical circuit concepts behind the different working modes of inverters and converters so as to enable deep understanding of their operation
2. To understand the various power quality issues
3. To discuss the need of non-conventional energy sources
4. To explain the role of embedded system in power electronics applications

Course Outcomes

At the end of the course students will be able to

1. Explain the operation of modern power converters such as DC-DC converters and multilevel inverters.
2. Explain the role of power electronics in Renewable Energy.
3. Equip with required skills to derive the criteria for the design of power converters for renewable energy applications
4. Explain the various terms related to power quality and systems that can be used to improve the power quality
5. Develop embedded controllers for power electronic based system.

Course Contents

Unit 1. Basic Devices in Power Electronics Systems **8 Hrs.**

Introduction to modern power semiconductor devices, its models and their selection for power electronics applications

Unit 2. Analysis and design of DC to DC converters

Basic concepts of Switched Mode power converters, Control of DC-DC converters, Buck converters, Boost converters, Buck-Boost converters, and Cuk converters, Full Bridge Converters, Control principle and application **8 Hrs.**

Unit 3. DC To Controlled AC: **10 Hrs.**

Controlled inversion, Full bridge inverter (VSI) with square controlled inversion switching, PWM control of VSI, current mode control of PWM VSI, current source PWM full Bridge inverter, pruning of harmonic profile, sine PWM inverter, control signal generation, 3phase full bridge inverter, Rectifier mode operation of inverter

Unit 4. Multilevel Inverters **10 Hrs.**

Multilevel voltage source inverters: two level voltage source inverter, cascaded H bridge multilevel inverter, diode clamped multilevel inverters,

flying capacitor multilevel inverter.

Unit 5. Power Electronics in Renewable Energy System **10 Hrs.**

Recent trends in energy consumption - World energy scenario - Energy sources and their availability - Qualitative study of different renewable energy resources: Solar, wind, Hydrogen energy systems, need to develop new energy technologies. Modelling of renewable energy sources- Wind Electric generators, Solar energy etc in MATLAB/PSCAD Simulink environment.

Unit 6. Typical functions microcontrollers in power electronic systems **10 Hrs.**

Measurement of voltage, current, speed, power and power factor, Frequency measurement, PWM implementation; Interfacing LCD Display, Keyboard Interfacing

Use of microcontroller in power converters: Overview of Zero Crossing Detectors, Generation of gating signals for Converters, Inverters and chopper circuit, Control of AC/DC electric drives

Reference Books

1. Power Electronics Circuit Devices & Applications, M.H Rashid, Pearson
2. Fundamental of Electrical Drives, Gopal K. Dubey, Narosa Publishing House
3. Power Electronics, Converters Applications and Design, N. Mohan, T. M. Undeland& W. P. Robbins, John Wiley and Sons,3rd Edition
4. P. T. Krein, "Elements of Power Electronics", OUP
5. John B. Peatman, "Design with PIC Microcontrollers", Pearson Education Asia
6. Power Electronics, M.D. Singh & K.B.Khanchandani, TMH
7. Rai G.D., "Non – Conventional Energy Sources", Khanna Publishers.
8. Modern power Electronics by P.C.Sen, S.Chand & Company

First Year M.Tech. Sem-II

ELL57*- Elective-III: ELL542-Advanced Image and Video Processing and Applications

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites- Advanced Digital Image Processing

Course Objectives

1. To study the wavelets in image processing and its applications

2. To learn the constraints in image processing when dealing with 3-D data sets
3. To understand the basics of Video processing and different techniques to estimate motion within a video sequence.
4. To Digital Video Processing Techniques and Applications
5. To learn the different Object Recognition algorithms.
6. To cover various real time applications of digital image processing

Course Outcomes

At the end of the course students will be able to

1. Discuss the wavelet technique and its applications in image processing
2. Illustrate the techniques in 3-D image processing.
3. Explain the concepts involved in video processing.
4. Describe the Digital Video Processing Techniques and Applications
5. Choose and apply suitable object Recognition algorithms based on application
6. Get broad exposure to and understanding of various applications of image processing in industry, medicine, and satellite image processing

Course Contents

Unit 1. Wavelets and Multiresolution processing: 10 Hrs.

Background, Multiresolution expansions: Series expansion, scaling function, wavelet function, Wavelets in 1-D: Expansion of functions, Multi-resolution analysis, Scaling functions, MRA refinement equation, Wavelet series expansion, Discrete Wavelet Transform (DWT), Continuous Wavelet Transform, Fast Wavelet Transform, Wavelet Transform in 2 dimension, Wavelet Packets. Applications of Wavelets in image processing.

Unit 2. 3-D Image Visualization 7 Hrs.

Sources of 3-D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiply connected surfaces, Image processing in 3D, Measurements on 3-D images.

Unit 3. Video Processing: 8 Hrs.

Fundamental Concepts in Video, Types of video signals, Analog Video, Digital Video, Color models in video, Video compression Techniques and standards H.261,H.263, MPEG1, MPEG2, MPEG4, MPEG7.

Unit 4. Digital Video Processing Techniques and Applications 8 Hrs.

Fundamentals of Motion Estimation and Motion Compensation, Motion Estimation Algorithms, Computational complexity, Video Enhancement and Noise Reduction, Case Studies: Object Segmentation and Tracking in the Presence of Complex Background, Content based video indexing

Unit 5. Object Recognition: 10 Hrs.

Patterns and Pattern Classes, Representation of Pattern classes, Types of classification algorithms: a) Recognition Based On Decision and Theoretic Methods - Minimum distance classifier, Correlation based classifier, Bayes classifier, Neural Networks, b) Recognition based on Structural method-tree classifier, Support Vector Machines

Unit 6. Applications of Image processing: 7Hrs

Space image processing, Medical/Biological image processing (interpretation of X-ray images, blood/cellular microscope images), Automatic character recognition (zip code, license plate recognition), Finger print/face/iris recognition, remote sensing: aerial and satellite image interpretations, Industrial applications

Reference Books

1. Fundamentals of Digital Image Processing", A. K. Jain, PHI.
2. Digital Image Processing "Willium K. Pratt Wiley, 3rd Edition.
3. Ardeshir Goshtas by, " 2D and 3D Image registration for Medical, Remote Sensing andIndustrial Applications", John Wiley and Sons,2005
4. M.Tekalp ,"Digital Video Processing" Prentice Hall USA,1995
5. The Image Processing Handbook, Fourth Edition, John C. Russ CRC Press 2002
6. Practical Image And Video Processing Using MatlabOge Marques Florida Atlantic University Wiley Publication (14 October 2011)

First Year M.Tech. Sem-II

ELL57*- Elective-III: ELL543: Advanced Process Control

Teaching Scheme	
Lectures	4 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Maths I, II, III, Signals and Systems, Control systems

Course Objectives

1. To understand process dynamics theory and modelling of various processes
2. To understand the dynamic behaviour of 1^{st} and 2^{nd} order process, state space and transfer function models along with MIMO process.
3. To learn about different process control models
4. To gain knowledge on the PLC and it's application real time problems
5. To learn on different feedback controller modes and their tuning for process control.
6. To understand the principle of cascade and advanced controllers

Course Outcomes

At the end of the course students will be able to

1. Explain the theory, process dynamics & modelling principles of various processes
2. Compare and differentiate the dynamic behaviour and characteristics of 1^{st}, 2^{nd} order processes, state space and also MIMO processes.
3. Explain the performance of different controller models
4. Apply the control using PLC for real time process problems
5. Analyse the performance of different feedback process controller modes and their tuning.
6. Summarize different types of cascade and advanced controllers

Course Contents

Unit 1. **Process dynamics & Mathematical modelling:** **9 Hrs.**

General modeling principle, Degree of freedom analysis, Dynamic model of representative process, Process dynamics & mathematical model, Transfer function model, Transfer function of simple models, Properties of transfer function, Linearization of non-linear model.

Unit 2. **Dynamic behaviour of first & second order process and characteristics of complicated process:** **6Hrs.**

Response of first order processes, Response of second order processes, Interacting & Non – interacting processes, State space & transfer function matrix models, Multiple input multiple output processes.

Unit 3. **Empirical model identification & development** **10 Hrs.**

Model development using linear & non-linear regression, Fitting first & second order models using step tests, Neural network models, Development of discrete time dynamic model, Identifying discrete time models from experimental data, Process reaction curve method, Statistical model identification

Unit 4. **Programmable logic controllers :** **09 Hrs.**

Architecture of PLC, Scanning consideration ladder diagrams, Timer & counter functions, Data handling functions, PLC programming functions: timer and counter functions, data handling functions, Advanced PLC functions: Analog PLC operations, PID control, Examples.

Unit 5. **Feedback Controller Principle:** **7Hrs.**

Block diagram of process feedback control, control performance measures for common input changes, Desired features of Feedback control, Discontinuous controller modes, continuous controller modes: Proportional, Integral and Derivative control modes, composite controller modes, PID Controller tuning for dynamic performance, Zeigler-Nichols closed loop tuning, Tuning and performance of feedback control systems, controller with two degree of freedom.

Unit 6. **Cascade Control and Model based control:** **9Hrs**

Cascade control design criterion, Cascade performance, Control algorithm & tuning implementation issues. Feed forward Controller**:** Design criterion, Feed forward performance, Control algorithm & tuning Implementation issues.

Model Based Control: internal model control (IMC) The smith predictor, Model predictive control (MPC),

Reference Books

1. "Process Dynamics & Control" – 3rd edition – EDGAR, DOYLE, WILEY.
2. "Process Control & Instrumentation", C D Johnson, PHI Publication
3. "Process control designing process & control systems for dynamics performances",Thomos Marlin, Tata McGraw Hill Publication
4. "Process control instrumentation handbook", Bela G Liptak

First Year M.Tech. Sem-II
ELL57*- Elective-III: ELL544-Wireless Adhoc & Sensor Network

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Wireless communication, Operating system and Networking

Course Objectives

1. To understand the principles of ad hoc wireless and sensor networks
2. To understand and design protocols including congestion control and routing
3. To design, analyze and simulate high-speed networks and assess performance.
4. To implement protocols using hardware/motes

Course Outcomes

At the end of the course students will be able to

1. The students understand the state of art techniques in wireless communication.
2. Students are enriched with the knowledge of present day technologies to enable them to face the world and contribute back as researchers.
3. Understand concepts of wireless communication

Course Contents

Unit 1. Adhoc Networks And Routing Protocols **9 Hrs.**

Ad hoc Wireless Networks – What is an Ad Hoc Network? Heterogeneity in Mobile Devices – Wireless Sensor Networks – Traffic Profiles – Types of Ad hoc Mobile Communications – Types of Mobile Host Movements – Challenges Facing Ad hoc Mobile Networks – Ad hoc wireless Internet . Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks – Classifications of Routing Protocols – Table–Driven Routing Protocols – Destination Sequenced Distance Vector (DSDV) – Wireless Routing

Protocol (WRP) – Cluster Switch Gateway Routing (CSGR) – Source–Initiated On–Demand Approaches – Ad hoc On–Demand Distance Vector Routing (AODV) – Dynamic Source Routing (DSR) –Temporally Ordered Routing Algorithm (TORA) – Signal Stability Routing (SSR) –Location–Aided Routing (LAR) – Power–Aware Routing (PAR) – Zone Routing Protocol (ZRP).

Unit 2. **Multicast Routing And Security** **09 Hrs.**

Issues in Designing a Multicast Routing Protocol – Operation of Multicast Routing Protocols – An Architecture Reference Model for Multicast Routing Protocols –Classifications of Multicast Routing Protocols : Tree–Based Multicast Routing Protocols, Mesh–Based Multicast Routing Protocols, Summary of Tree and Mesh based Protocols : Energy Efficient Multicasting, Multicasting with Quality of Service Guarantees, Application Dependent Multicast Routing, Comparisons of Multicast Routing Protocols, Design Goals of a Transport Layer Protocol for Ad hoc Wireless Networks, Classification of Transport Layer Solutions,TCP over Ad hoc Wireless Networks, Security in Ad Hoc Wireless Networks: Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks: Key Management ,Secure Routing in Ad hoc Wireless Networks.

Unit 3. **QoS And Energy Management** **7 Hrs.**

Issues and Challenges in Providing QoS in Ad hoc Wireless Networks , Classifications of QoS Solutions: MAC Layer Solutions , Network Layer Solutions, QoS Frameworks for Ad hoc Wireless Networks, Energy Management in Ad hoc Wireless Networks: Introduction, Need for Energy Management in Ad hoc Wireless Networks, Classification of Energy Management Schemesm: Battery Management Schemes,Transmission Power Management Schemes , System Power Management Schemes.

Unit 4. **Sensor Networks – Architecture and MAC Protocols** **8Hrs.**

Single node architecture : Hardware components, energy consumption of sensor nodes, Network architecture: Sensor network scenarios, types of sources and sinks, single hop versus multi-hop networks, multiple sinks and sources, design principles, Development of wireless sensor networks, physical layer and transceiver design consideration in wireless sensor networks, Energy usage profile, choice of modulation, Power Management - MAC protocols – fundamentals of wireless MAC protocols, low duty cycle protocols and wakeup concepts, contention-based protocols, Schedule-based protocols - SMAC, BMAC, Traffic-adaptive medium access protocol (TRAMA), Link Layer protocols :fundamentals task and requirements, error control, framing, link management.

Unit 5. **Sensor Networks – Routing Protocols** **05 Hrs.**

Gossiping and agent-based uni-cast forwarding, Energy-efficient unicast, Broadcast and multicast, geographic routing, mobile nodes, Data-centric routing: SPIN, Directed Diffusion, Energy aware routing, Gradient-based routing: COUGAR, ACQUIRE, Hierarchical Routing: LEACH,

PEGASIS, Location Based Routing:GAF, GEAR, Data aggregation – Various aggregation techniques.

Unit 6 **4 Hrs.**

Sensor Networks -Operating Systems :
Introduction to TinyOS – NesC, Interfaces, modules, configuration, Programming in TinyOS using NesC, Emulator TOSSIM.

Reference Books

1. C. Siva Ram Murthy and B. S. Manoj, "Ad Hoc Wireless Networks Architectures and Protocols", Prentice Hall, PTR, 2004.
2. C. K. Toh, "Ad Hoc Mobile Wireless Networks Protocols and Systems", Prentice Hall, PTR, 2001.
3. C.S.Raghavendra Krishna, M.Sivalingam and Taribznati, "Wireless Sensor Networks", Springer publication, 2004.
4. HolgerKarl , Andreas willig, "Protocol and Architecture for Wireless Sensor Networks", John wiley publication, Jan 2006.
5. K.Akkaya and M.Younis, " A Survey of routing protocols in wireless sensor networks", Elsevier Adhoc Network Journal, Vol.3, no.3,pp. 325-349, 2005.
6. . I.F. Akyildiz, W. Su, Sankarasubramaniam, E. Cayirci, "Wireless sensor networks: a survey", computer networks, Elsevier, 2002, 394 - 422.
7. . Jamal N. Al-karaki, Ahmed E. Kamal, "Routing Techniques in Wireless sensor networks: A survey", IEEE wireless communication, December 2004, 6 – 28.

First Year M.Tech. Sem-II
ELL58*- Elective-IV: ELL 545-Artificial Neural Networks

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Engineering Maths

Course Objectives

1. To understand basic neural network models and basic learning algorithms.
2. Design and apply neural systems for various applications.

Course Outcomes

At the end of the course students will be able to

1. Develop the skills to gain a basic understanding of neural network theory.
2. Explore the functional components of neural network classifiers or controllers
3. Learn the detailed theoretical and mathematical basics of various algorithms.
4. Design and analyses of neural network for various applications.

Course Contents

Unit 1.	**Fundamental Concepts and Models of Artificial Neural Systems** Biological Neurons and Their Artificial Models, models of artificial neural networks, Neural processing, Learning and adaptation, Neural Network learning rules, Overview of neural networks	**6 Hrs.**
Unit 2.	**Single Layer Perceptron Classifiers** Classification model, features and decision regions, Discriminant functions, Linear machines and minimum distance classifications, Nonparametric training concept, training and classification using the discrete perceptron algorithm and example, Single layer continuous perceptron networks for linearly separable classification,. Multi category Single layer perceptron networks.	**8 Hrs.**
Unit 3.	**Multi Layer Feed Forward networks** Linearly non separable pattern classification, Delta learning rule for multi perceptron layer, Generalized delta learning rule, Feed forward recall and error back propagation training , Learning factors, Classifying and expert layered network, Functional link networks	**6 Hrs.**
Unit 4.	**Single Layer Feed Forward networks** Basic concept of dynamical systems, Mathematical foundation of discrete time Hopfield networks, Mathematical foundation of gradient type Hopfield network, transient response of continuous time networks, relaxation modeling in single layer feedback network, example solution of optimization problem	**7 Hrs.**
Unit 5.	**Matching & self organizing networks** Hamming net & MAXNET, unsupervised learning of clusters, counter propagation network, feature mapping, self organizing feature maps, cluster discovery network (art1)	**7 Hrs.**
Unit 6	**Applications of Neural algorithms & systems** Linear programming modeling network, character recognition network, neural networks control applications, networks for robot kinematics, connectionist expert systems for medical diagnosis, self organizing semantic maps	**6 Hrs**

Reference Books

1. Simon Haykin, "Neural Networks: A comprehensive foundation", Second Edition, Pearson Education Asia.
2. Robert J. Schalkoff, "Artificial Neural Networks", McGraw-Hill International Editions, 1997.
3. Jacek M. Zurada "Introduction to artificial neural systems".
4. Kishan Mehrotra, Chilukuri K. Mohan, Sanjay Ranka, "Element of artificial neural networks", 2nd edition, 2010.
5. B. Yegnanarayana "Artificial Neural networks"

First Year M.Tech. Sem-II
ELL58*- Elective-IV: ELL546-VLSI in Digital Signal Processing

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: VLSI Design and Digital Signal Processing

Course Objectives

1. To discuss the timing issues and clock synchronization of digital circuits.
2. Design and analysis the structure of arithmetic blocks, data path and memory units.
3. To understand the different algorithms for DFG and iteration bound.
4. Study and understand the Pipelining and parallel processing for the digital filters.
5. Study and understand Retiming techniques and Unfolding concepts.

Course Outcomes

At the end of the course students will be able to

1. Understand the clock issues in synchronous digital circuits like clock skew, Jitter, clock distribution, latch based clocking.
2. Design and analyze the arithmetic building blocks and memory structure efficiently.
3. Representation of data flow graph and iteration boundfor computing speed and power by certain algorithms.

4. Distinguish between pipelining and parallel processing.
5. Understand the retiming for minimization and unfolding for bit level parallel processing.

Course Contents

Unit 1. **Timing issues in Digital Circuits** **7 Hrs.**

Timing Classification of Digital Circuits, Synchronous Design (Clock Skew, Jitter, Clock Distribution, Latch Based Clocking), Self-Timed Circuits Design (An Asynchronous Techniques), Synchronizers and Arbiters Using PLL for Clock Synchronization, DLL.

Unit 2. **Designing Arithmetic Building Blocks and their analysis** **6 Hrs.**

Adders, Multipliers, Shifters, Power and Speed Trade-Off in Datapath Structures

Unit 3. **Designing Memory and Array Structures** **7 Hrs.**

Introduction, The Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation In Memories.

Unit 4. **DFG representation and Iteration Bound** **7 Hrs.**

DFG, loop bound and iteration bound, Algorithm for computing iteration bound, (Longest path algorithm, Minimum cycle algorithm), Iteration bound for multirate DFGs.

Unit 5. **Pipelining and Parallel Processing** **7 Hrs.**

Pipelining for FIR digital filters, Data broadcast structures, Fine grain pipelining, Parallel processing, Pipelining and parallel processing for low power, Combining pipelining and parallel processing, Systolic architecture.

Unit 6. **Retiming and Unfolding** **9 Hrs**

Retiming: Definitions and properties, Solving system of inequalities, Retiming techniques (cutset retiming and pipelining, Retiming for clock period minimization, Retiming for register minimization

Unfolding: Concept behind unfolding, an algorithm for unfolding, Properties for unfolding, Applications for unfolding, Sample period reduction, Word level parallel processing, bit-level parallel processing

Reference Books

1. Keshab K. Parhi, VLSI Digital Signal Processing Systems, Wiley Publications
2. "Digital design processing: - Principles, algorithms and application", John. G Proakis, PHI Publication.
3. "Digital Design Principles and Practices (Edition II)", John F. Wakerly, PH Inc.

First Year M.Tech. Sem-II
ELL58*- Elective-IV: ELL 547-Cryptography and Network Security

Teaching Scheme	
Lectures	3 Hrs. /Week
Tutorial	1 Hr/Week
Total Credits	4

Evaluation Scheme	
SE-I	25
SE-II	25
SEE	50
Total	**100**

Prerequisites: Computer Communication Network, Wireless Network

Course Objectives

1. Understand security concepts, Ethics in Network Security
2. Understand security threats, and the security services and mechanisms to counter them
3. Comprehend and apply relevant cryptographic techniques
4. Comprehend security services and mechanisms in the network protocol stack
5. Comprehend and apply authentication services and mechanisms
6. Comprehend and apply relevant protocol like SSL, SSH etc.

Course Outcomes

At the end of the course students will be able to

1. Identify network security threats and determine efforts to counter them
2. Write code for relevant cryptographic algorithms.
3. Write a secure access client for access to a server
4. Send and receive secure mails
5. Determine firewall requirements, and configure a firewall.

Course Contents

Unit 1. **Introduction** **7 Hrs.**

Need of security, security services, Active vs. Passive attacks, OSI Security Architecture, one time passwords, A Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques

Unit 2. **Number Theory** **7 Hrs.**

Introduction to Number Theory, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3. **Private-Key (Symmetric) Cryptography** **7 Hrs.**

Block Ciphers, Stream Ciphers, and RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4. **Public-Key (Asymmetric) Cryptography** **7 Hrs.**

RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 5. **Authentication, IP and Web Security** **8 Hrs.**

Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, X.509 Digital Certificate Standard, Authentication service, Internetworking and Internet protocols: IPv4, IPv6, IP security Architecture, Authentication Header, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6. **System Security** **8 Hrs**

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems

Reference Books

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, Third Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network security, Private communication in a Public World".

3. V. K. Pachghare "Cryptography and Information Security", PHI.
4. Christopher M. King, "Security architecture, design deployment and operations", Curtis Patton and RSA Press.
5. Stephen Northcatt, LenyZeltser, "Inside network Perimeter Security", Pearson Education Asia.

First Year M.Tech. Sem-II
ELP548: Real Time Embedded System Design Lab

<table>
<tr><th colspan="2">Teaching Scheme</th><th colspan="4">Evaluation Scheme</th></tr>
<tr><td>ELL539: Practical</td><td>2 Hrs. /Week</td><td rowspan="3">CIE</td><td colspan="2">ELL539</td><td>50</td></tr>
<tr><td rowspan="2">ELL541:Tutorial</td><td rowspan="2">1Hr/week</td><td colspan="2">ELL541</td><td rowspan="2">50</td></tr>
<tr><td colspan="2">ELL57*</td></tr>
<tr><td rowspan="3">ELL57*: Tutorial</td><td rowspan="3">1Hr/week</td><td rowspan="3">SEE</td><td>ELL539</td><td>POE</td><td>25</td></tr>
<tr><td>ELL541</td><td rowspan="2">Comprehensive Viva voce</td><td rowspan="2">25</td></tr>
<tr><td>ELL57*</td></tr>
<tr><td>Total Credits</td><td>2</td><td colspan="3">Total</td><td>150</td></tr>
</table>

Note : ELP548: Consists of **Real Time Embedded System Design Lab: POE e**xternal exam will be conducted for **ELL539 and Comprehensive Viva voce for ELL541 and offered elective ELL57***

List of Experiments: ELL539: Real Time Embedded System Design

Experiments based on following things using VxWorks RTOS or uCOS-II OS

1. Timing
   a) Vary the number of ITERATIONS in the loop(300,400,500,600,700) and note the changes in execution speed.
   b) Decrease the number of the iteration to 5, note what happens(you should get a warning message). Write a program to get the timing in this case.
2. Multitasking
   a) Up to a ten integer arguments can be passed to a task during the call to *taskSpawn()*. Pass a unique argument to each of the ten tasks and have them print it.
3. Semaphore
   a) Study of Binary Semaphore.

b) Study of different Semaphore functions such as *semBCrete, semMCreate, semCCreate, semTask, semDelete, semTake, semGive*

4. Message Queue

a) Send different messages by using *msgQCreate, msgQDelete, msgQSend, msgQReceive*

5. Round Robin Task Scheduling

a) Write the source code necessary to vary the time of TIMESLICE(10,20, 30,40,50,60,120,180,240 and 300 clock ticks).

9. Find the scheduling by running dummy task

10. Calculate EDF (Earliest Deadline First) Scheduling

ELP558: Real Time Embedded System Design Lab-Comprehensive Viva voce				
Teaching Scheme			**Evaluation Scheme each for ELL541 and ELL57***	
Tutorial	ELL541 : 1Hrs. /Week	CIE	**ELL541**	25
	ELL57*: 1hr/week		ELL57*	25
Total	2	SEE		25
		Total		**75**

Note: Real Time Embedded System Design Lab consists of Comprehensive viva voce –ELL 541:PES and ELL57*:Elective-III

First Year M.Tech. Sem-II
ELP549: Analog & Mixed Mode VLSI Circuits Lab

Teaching Scheme			**Evaluation Scheme**		
ELL540: Practical	2 Hrs. /Week	CIE	ELL540		50
			ELL58*		
ELL58*: Tutorial	1Hr/week	SEE	ELL540	POE	25
			ELL58*	Comprehensive Viva voce	25
Total Credits	**2**	**Total**			**150**

List of Tutorial/experiments- ELL540: Analog & Mixed Mode VLSI Circuits

PART – A

Digital design

1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with the technological library, Do the initial timing verification with gate level simulation.
    1. An inverter
    2. Basic/universal gates
    3. Flip flop - RS, D, JK, MS, T
    4. Successive approximation register [SAR]

PART - B

Analog design

1. Design an Inverter with given specifications, completing the design flow mentioned below:
    a. Draw the schematic and verify the following:
        i) DC Analysis ii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS
    d. Extract RC and back annotate the same and verify the Design
    e. Verify & Optimize for Time, Power and Area to the given constraint

2. Design the following circuits with the given specifications, completing the design flow mentioned below:
    a. Draw the schematic and verify the following: i) DC Analysis ii) AC Analysis
        iii) Transient Analysis
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS
    d. Extract RC and back annotate the same and verify the Design.

3. Design an op-amp with the given specification using given differential amplifier, Common source and Common Drain amplifier in library and completing the design flow as mentioned below:
    a. Draw the schematic and verify the following:
    b. Draw the Layout and verify the DRC, ERC
    c. Check for LVS

i) DC Analysis ii) AC Analysis iii) Transient Analysis

d. Extract RC and back annotate the same and verify the Design

4. Design a 4 bit R-2R based DAC for the given specification and completing the design flow mentioned using given op-amp in the library.

a. Draw the schematic and verify the following:

i) DC Analysis ii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC

c. Check for LVS.

Comprehensive viva voce

Comprehensive Viva Voce will be carried out by Internal and External examiners as oral examination for the offered ELL58* -Elective-I subject (**ELL545, ELL546, and ELL547)**

First Year M.Tech. Sem-II
ELD550: Seminar/Mini Project/Training

Teaching Scheme	
Practical	2 Hr/student
Total Credits	2

Evaluation Scheme	
CIE	100
SEE	-
Total	**100**

Course Objectives

1. To make the student to know about his interest field
2. To understand the focussing and summing ability
3. To develop the attitude towards research
4. To give an insight into forming problem statement
5. To improve the presentation skills

Course Outcomes

At the end of the course students will be able to

1. Appropriate and select seminar topic in his field of interest
2. Comprehend and summarise the topic studied
3. Analyse the topic and will explore further
4. Formulate the problem statement
5. Show improvement in confidence level

Seminar-II/Mini Project/ Training:

The students shall compulsorily choose one of the three subjects i.e.,Seminar-II or Mini Project or industrial Training for 2 credits

Seminar II:

Each student will be required to prepare a Seminar and present a Seminar on a topic in any of the areas of modern technology related to Electronics Engineering including interdisciplinary fields. The topic/title will be chosen by the student in consultation with the Faculty Advisor allocated to each student. The topic may be related to the project that is to be carried out in second year or it may be an independent topic. The student will be required to submit the Seminar Report and present a talk to an audience of Faculty/Students in open defence in front of the Seminar Evaluation Committee having Faculty Advisor as one of its members. The Head of Department will constitute the Seminar Evaluation Committee.

Or Mini Project:

1. The project needs to encompass the concepts leant in a courses in the previous/current semesters, so that the student will learn to integrate, the knowledge acquired to provide a solution to the defined problem statement of the mini-projects.
2. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
    a. Embedded systems
    b. VLSI design
    c. Signal Processing
    d. Image processing, video processing
    e. Automation
    f. ARM controllers
    g. Communications
    h. Networking
3. Time plan: Effort to do the project should be between 40 hours,

Or Industrial Training:

Student shall take the training in industry/research laboratories for a minimum period of 20-25 days (including training period, preparation of training report and presentation) after the end of 1st semester and shall produce the report on the same to the concerned guide for evaluation. Candidates in consultation with the guides shall carryout literature survey / visit to Industries to finalize the topic of dissertation. Evaluation of the same shall be taken up during end of II Semester by the department committee.

Continuous internal evaluation: CIE

Continuous evaluation of the seminar/mini project shall be made by dissertation monitoring committee members including guide. The student is required to present seminar/ demo and this will be evaluated for 100 marks. It includes submission of the seminar/mini project/industrial training report, presentation of seminar /training report /demonstration of the mini-projects and viva-voce conducted by internal dissertation committee.